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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,610	12/31/2003	Darvin R. Edwards	TI-36608 (032350.B566)	8535

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,610	EDWARDS, DARVIN R.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-22,25-34 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-22* is/are allowed.

6)☒ Claim(s) *25-27,29-34 and 36* is/are rejected.

7)☒ Claim(s) *25 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The examiner thanks Applicant for the clear explanations of "contacting " and "contacting without adhering" as used in the claims. Applicant states that it is well known in the art that many common solder materials adhere well to metallic surfaces of common heat sinks but do not adhere well to bare silicon surface of common silicon chips (Remark filed 03/10/2005, page 6). As such, a common solder material such as a solder material disclosed by the '078 patent (column 5, Table 1), disclosed by the '668 patent (column 1, lines 52-57), by the '730 publication (paragraph [0023]), a common heat sink, and a common silicon chip disclosed by these references meet the mentioned limitations.

2. **New claim 28** has the same numerical reference as amended claim 28, therefore new claim 28 has been relabeled as **claim 36**.

3. **Claim 28** is objected to because of the following informalities: claim 28 recites: "is the bonded to the die" which is not clear. As best as can be understood, the phrase should be "is bonded to the die". Appropriate correction is required.

4. **Claim 25** is objected to because of the following informalities: claim 25 recites: "a semiconductor die" and "the chip" which is not clear. As best as can be understood, "the chip" is the same as "the semiconductor die".

5. **Claim 28** is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Specifically, claim 28, which depends on claim 25, recites: "a glue layer with which the lid with the conductive layer is bonded to the die", whereas claim 25 recites "the conducting layer...contacting ..the top surface of the semiconductor die". In other words, claim 28, dictating that a glue layer (best seen as the portion of the "bonding layer" 260 between the rightmost semiconductor die 240 and the conducting layer 250 of Fig. 2A) is between the lid with the conductive layer and the semiconductor die, fails to limit that the lid with the conductive layer contacts the semiconductor die.

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. **Claims 25, 29-31, 33, and 36** are rejected under 35 U.S.C. 102(e) as anticipated by Sur et al. U.S. Patent 6,724,078 (the '078 patent).

The '078 patent discloses in Figures 2-4 and respective portions of the specification a system as claimed.

Referring to **claims 25 and 35**, the '078 patent discloses a system comprising:

a semiconductor die (silicon semiconductor 50) having a bottom surface and a top surface;

a lid (52, a common heat sink) with a cavity (no number) having a inner surface (no number), accommodating the semiconductor die (as is evident from Fig. 2); and

a heat conducting layer (60, a common solder) having a thermal conductivity greater than 10 W/m-°C (column 5, Table 1) adhering to the inner surface of the cavity and substantially conforming to the surface contour of the top surface of the semiconductor die and contacting (Fig. 2, and see note above for the interpretation of contacting and contacting without adhering) without adhering to the top surface of the semiconductor die.

Referring to **claim 29**, as mentioned above, the '078 patent discloses that the heat conductive material is a solder material.

Referring to **claims 30 and 31**, column 5, Table 1, discloses that the solder material comprises lead or is substantially free of lead (when the solder material is formed of a material other than lead).

Referring to **claim 33**, although not explicitly disclosed by the '078 patent, the thermal conductivity of the heat conductive material (solder 60/88) is higher than the thermal conductivity of epoxies (as is admitted by Applicant, and as is known in the art which is disclosed by Back et al. U.S. Patent 6,756,668 (the '668 patent) in column 1, lines 52-57 and cited here only for the purpose of record keeping).

Referring to **claim 36**, the '078 patent further discloses a substrate (54) to which the lid (52) is adhered.

8. **Claims 25, 29-31, 33, and 36** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '668 patent.

The '668 patent discloses in the Background Art Section and in Fig. 2 a system comprising:

a semiconductor die (silicon semiconductor die 20) having a bottom surface and a top surface;

a lid (40, a common heat sink, column 1, lines 40: "having a good heat emissive capacity") with a cavity (48) having a inner surface (42), accommodating the semiconductor die (as is evident from Fig. 2); and

a heat conducting layer ("thermal interface material", or TIM 60) having a thermal conductivity greater than 10 W/m-°C (column 1, lines 52-57. a common solder) adhering to the inner surface of the cavity and conforming to the surface contour of the top surface of the semiconductor die and contacting without adhering to the top surface of the semiconductor die (see notes above for the interpretation of "adhering" and "without adhering").

Referring to **claim 29**, as mentioned above, the reference discloses that the heat conductive material is a common solder material.

As for the limitations and materials of **claims 30-31**, they are known and available to one of ordinary skill in the art as disclosed by the references cited thus far, for example, Table 1 of the '078 patent.

Referring to **claim 36**, the reference further discloses a substrate (12) to which the lid (40) is adhered.

9. **Claim 32** is rejected under 35 U.S.C. §103(a) as being unpatentable over the '078 patent in view of the '712 publication.

The '078 patent discloses a system as claimed and as detailed above including the conductive layer 60 formed of a common solder of various materials as claimed in claims 29-31 and as detailed above, but fails to disclose that the conducting layer could be a thermoplastic material. The '712 publication, in disclosing a conductive layer ("thermal interface") used between lid/heat sink and IC (Abstract) similarly to the present invention's and the '078 patent's, teaches that the conductive layer formed of a thermoplastic material ("thermal setting epoxy", paragraph [0001]) provides long term reliability, high thermal conductivity, low thermal resistance, low shrinkage, among other advantages (paragraph [0029]). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a thermoplastic material to form the '078 patent's conductive layer. One would have been motivated to make such a modification in view of the teachings by the '712 publication that the conductive layer formed of a thermoplastic material provides long term reliability, high thermal conductivity, low thermal resistance, and low shrinkage.

10. Claims 25-27, 29-31, 33-34, and 36 are rejected under 35 U.S.C. §103(a) as being unpatentable over Edwards et al. U.S. Patent 5,819,402 (the '402 patent) in view of the '730 publication.

The '402 patent discloses in Figs. 1-3 a system comprising a silicon semiconductor die (51) having a bottom surface and a top surface; a lid ("cap" or common heat sink 50) with a cavity (no number) having a inner surface (no number), accommodating the semiconductor die (as is evident from the figures); and a heat conducting element (71) adhering to the inner surface of the cavity and conforming to the surface contour of the top surface of the semiconductor die

and contacting the top surface of the semiconductor die. The '402 patent further discloses that the heat conducting element contacts an edge of the die (as is evident from the figures and in reference to **claim 26**), that the lid has two or more cavities that accommodate two or more dies (**claim 27**), and that the heat conductive material in the cavities varies in thickness (as is evident from the figures) to compensate for any variation in die-thickness (column 7, lines 40-45, in reference to **claim 34**). The '402 patent further discloses the advantage of re-workability of the system (column 8, lines 6-10).

However, the '402 patent fails to disclose that the heat conducting element (or as appropriately called thermal interface material (TIM) in the art as it is located between the thermally conductive lid and the thermally generating die for facilitating dissipating harmful thermal energy from the die to the environment) has a thermal conductivity greater than 10 W/m-°C and further appears failing to disclose that the TIM does not adhere to the top surface of the semiconductor die (as the '402 teaches using a thermal paste for the TIM, the TIM appears to adhere to the top surface of the semiconductor die).

The '730 publication, in also disclosing a TIM between a semiconductor die and a lid having a cavity, teaches that a variety of phase change materials, particularly the common solder material made up entirely of a fusible thermally conductive solder material, such as In, In/Sn, In/Ag, Sn/Ag/Cu, Sn/Bi, In/Sn/Bi and In/Zn, Sn/Ag and Sn/In/Ag (paragraph [0023]), which is pre-attached to a surface of the cavity of the lid using a **heat treatment** (Fig. 5b and paragraph [0027]) – which meets the limitation "adhering to the inner surface of the cavity" – and which remains **solid** during the normal operation of the semiconductor die (paragraph [0019], which meets the property "contacting without adhering to the top surface of the semiconductor die ",

enables application at the post-manufacturing step (paragraph [0006]: "it is necessary for the customer to obtain the thermal interface material or have it on hand so that it can be applied between the heat spreader and the semiconductor die", or application versatility for short). Note that although the '730 publication does not explicitly disclose a thermal conductivity greater than 10 W/m-°C, the TIM formed of a common solder material inherently possess the limitation. See for example, the '668 patent, column 1, lines 52-57, cited above.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '402 patent's system using the TIM taught by the '730 publication. One would have been motivated to make such a modification in view of the teachings by the '730 publication that TIM formed of common solder materials, which also meet the limitations of **claims 29-31, 33, and 36**, pre-attached to the inner surface of the cavity of the lid with a heat treatment, offers application versatility, which works in concert with the stated re-workability by the '402 patent. Note also that one still has to determine the thickness of the heat conductive material in each of the cavities of the modified device to compensate for any variation in die-thickness, but that would be within the skill of one in the art at the time the invention was made.

11. Applicant's arguments with respect to claims 25-27, 29-34, and 36, filed 03/10/2005, have been fully considered but they are not persuasive.

With respect to Applicant's argument on page 9 that Sur (the '078 patent) teaches depositing an "adhesion metal layer" (82), (which adheres to the surface of the semiconductor die 50, which prevents the disclosure from meeting the limitation "contacting without adhering

to the top surface of the semiconductor die" of claim 25 – a situation so similar to the amended claim 28), it is respectfully pointed out that the embodiment of Fig. 2 does not use such an adhesion metal layer.

With respect to Applicant's argument on page 10 that Baek (the '668 patent) teaches a silicon semiconductor package that includes a thermal interface material (TIM) with voids, it is respectfully pointed out that the structure and disclosure thereof that the examiner relies on is the prior art Fig. 2 disclosed by the '668 patent.

With respect to Applicant's argument on pages 11-12 that that Edwards (the '402 patent) fails to teaches a heat conducting layer that contacts but does not adhere to the top surface of the semiconductor die, it is respectfully pointed out that the structure and disclosure thereof that the examiner relies on is the '402 patent's package, which comprises a plurality of silicon semiconductor dies and a common heat sink, using the common solder materials taught by the '730 publication, as detailed above. The structure thus disclosed, comprising silicon semiconductor dies, a common heat sink, and a common solder material (the heat conducting layer), enabling the heat conducting solder material to contact but not to adhere to the top surface of the semiconductor die, as explained by Applicant and as agreed upon by the examiner as detailed above in paragraph numbered 1.

Allowable Subject Matter

12. **Claims 15-22** are allowable over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or render obvious a system for dissipating heat from a

semiconductor device with all limitations as recited in claim 15, characterized in that the first die has a first thickness and the second die has a different second thickness, and that the conductive layer is formed such that the thickness of the first die and the conductive layer on top of the first die is substantially equal to the thickness of the second die and the conductive layer on top of the first die.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
April 13, 2005

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